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December 28, 1999

BOX: PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Application of **Tae-yong SOHN**
APPARATUS AND METHOD FOR SELECTIVELY CONVERTING CLOCK FREQUENCY IN DIGITAL SIGNAL RECEIVER
Our Reference: Q57124

Dear Sir:

Attached hereto is the application identified above including the specification, claims, three (3) sheets of drawings and one (1) priority document. **The requisite U.S. Government Filing Fee, executed Declaration and Power of Attorney and Assignment will be submitted at a later date.**

The Government filing fee is calculated as follows:

Total Claims	11 - 20 =	0 x $18 =	$ 000.00
Independent Claims	3 - 3 =	0 x $78 =	$ 000.00
Base Filing Fee	($760.00)		$ 760.00
Multiple Dep. Claim Fee	($260.00)		$ 000.00
TOTAL FILING FEE			**$ 760.00**

Priority is claimed from:

Korean Patent Application	Filing Date
98-59415	December 28, 1998

Respectfully submitted,
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APPARATUS AND METHOD FOR SELECTIVELY CONVERTING CLOCK FREQUENCY IN DIGITAL SIGNAL RECEIVER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a digital signal receiver, and more particularly, to an apparatus for selectively converting clock frequency in a digital signal receiver, which detects a frame rate of an input signal and provides a clock frequency corresponding to the frame rate.

Description of the Related Art

In a digital television (TV) broadcast, signals transmitted from a broadcasting station to a TV receiver as well as the signals within a TV are all digital signals, so that a more distinct image and clearer sound can be produced as compared to the case of using analog signals. Digital TV can provide images in any of 18 video broadcast standards, from the standard TV (SDTV) scheme having a 640×480 resolution which is the same as that of the conventional analog NTSC (National Television System Committee) scheme, to a high definition television (HDTV) scheme having a 1920×1080 resolution which is seven times that of the SDTV scheme. Also, digital TV adopts a DOLBY AC-3 scheme to reproduce a clear stereophonic sound.

Digital TV also utilizes a highly efficient data compression technology with a compression ratio which is higher than 50:1, so that a broadcasting station can provide more channels. Also, since digital TV allows bidirectional transmission, digital TV provides quite different services than those provided in analog TV.

FIG. 1 is a block diagram of a digital TV receiver. The digital TV receiver of FIG. 1 includes an antenna 100, a tuner 102, an intermediate frequency (IF) module 104, a channel decoder 106, a transport stream (TS) decoder 108, an audio decoder 110, an audio signal processor 112, a speaker 114, a video decoder 116, an on-screen graphic mixer (OSGM) 118, a video signal processor 120, a cathode ray tube (CRT) 122 and a microprocessor 124.

The tuner 102 selects one radio frequency (RF) channel from a broadcasting signal received via an antenna 100, under the control of a microprocessor 124. The IF module 104 receives the IF frequency from the tuner 102 and converts the IF

signal to a baseband signal. The channel decoder 106 channel-decodes the baseband signal from the IF module 104 to produce a data bit stream. The TS decoder 108 separates audio data, video data and additional data from the data bit stream from the channel decoder 106. The audio decoder 110 receives the audio data and decodes the audio data according to the MPEG standard or Dolby AC-3 standard, and the audio signal processor 112 outputs the decoded audio signal to the speaker 114.

The video decoder 116 receives the video data from the TS decoder 108 and decodes the video data according to the MPEG standard, and the OSGM 118 mixes OSG data and the decoded video data under the control of the microprocessor 124. The video signal processor 120 receives the signal from the OSGM 118, processes the signal, and then outputs the processed signal to the CRT 122.

The digital TV receiver having the above structure may have an extra tuner for an analog signal. The American Television System Committee (ATSC) standard, a type of digital broadcasting scheme, adopts various frame rates for a digital signal, including 60 Hz, 59.94 Hz, 30 Hz, 29.94 Hz, 24 Hz and 23.97 Hz. Thus, it is necessary to convert the clock frequency of the digital TV receiver selectively according to the frame rate of the digital signal, thereby preventing omission or redundancy in signal processing.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an apparatus and method for selectively converting a clock frequency of a digital signal receiver, which corresponds to the frame rates of incoming digital signals.

To achieve the object of the present invention, there is provided an apparatus for converting a clock frequency in a digital signal receiver, comprising: a first phase locked loop (PLL); a second phase locked loop; a switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal; and a controller for controlling the switching portion to select and output the clock frequency corresponding to the frame rate of an input digital signal.

Preferably, the first phase locked loop generates a clock frequency of 74.25 MHz and the second phase locked loop generates a clock frequency of 74.175 MHz.

Additionally, it is preferred that when the frame rate of the input digital signal is 60 Hz, 30 Hz or 24 Hz, the controller controls the switching portion to select the clock frequency from the first phase locked loop, and when the frame rate of the input digital signal is 59.94 Hz, 29.97 Hz or 23.97 Hz, the controller controls the switching portion to select the clock frequency from the second phase locked loop.

BRIEF DESCRIPTION OF THE DRAWINGS

The above object and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a block diagram of a digital television (TV) receiver;

FIG. 2 is a block diagram of a digital TV receiver having a clock frequency converting apparatus according to the present invention; and

FIG. 3 is a detailed circuit diagram of the phase locked loop (PLL) of FIG. 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In FIG. 2, which shows a digital signal receiver having a clock frequency converting apparatus according to the present invention, reference numeral 200 represents a transport stream (TS) decoder, reference numeral 202 represents a video decoder, reference numeral 204 represents an analog-to-digital converter (ADC), reference numeral 206 represents a format converter, reference numeral 208 represents a phase locked loop (PLL), reference numeral 210 represents a buffer, reference numeral 212 represents a controller, reference numeral 214 represents an on screen graphic mixer (OSGM), and reference numeral 216 represents an oscillator.

The ADC 204 converts an analog NTSC signal to a digital signal. The format converter 206 converts the video data VIDEO from the video decoder 202 and the video data VIDEO from the ADC 204 into a predetermined display format. The PLL 208 includes first and second PLLs which generate different clock frequencies, and outputs a clock frequency selected under the control of the controller 212.

The controller 212 detects the frame rate from the format converter 206 and controls the PLL 208 such that the clock frequency which corresponds to the detected frame rate is output from the PLL 208. In particular, when an analog NTSC signal is input, the controller 212 controls the buffer 210 connected to the PLL 208

such that the clock frequency is applied only to blocks associated with processing the analog NTSC signal. That is, when video data is being received via the ADC 204, it is unnecessary to provide a clock frequency CLOCK to the video decoder 202. Thus, the controller 212 controls the buffer 210 such that the clock frequency is provided only to the format converter 206 and the OSGM 214.

FIG. 3 is a detailed circuit diagram of the PLL 208 of FIG. 2. As shown in FIG. 3, the PLL 208 includes a first PLL 208a, a second PLL 208b and a switching portion 208c. The first PLL 208a includes a phase comparator 302, a low pass filter 304, a voltage controlled oscillator (VCO) 306 and a frequency divider of 1/N 308. The second PLL 208b includes a phase comparator 402, a low pass filter 404, a VCO 406 and a frequency divider of 1/N 408. In this embodiment, the first PLL 208a generates a clock frequency of 74.25 MHz and the second PLL 208b generates a clock frequency of 74.175 MHz. The switching portion 208c selectively outputs the clock frequency of 74.25 MHz or 74.175 MHz according to a selection signal from the controller 212.

The various frame rates of a digital signal according to the ATSC standard, including 60 Hz, 59.94 Hz, 30 Hz, 29.94 Hz, 24 Hz and 23.97 Hz, are classified into one of two groups: a first group including 60 Hz, 30 Hz and 24 Hz, and a second group including 59.94 Hz, 29.94 Hz and 23.97 Hz.

When an input digital signal has a frame rate which is included in the first group, the controller 212 controls the switching portion 208c to selectively output the clock frequency of 74.25 MHz from the first PLL 208a. Meanwhile, when an input digital signal has a frame rate which is included in the second group, the controller 212 controls the switching portion 208c to selectively output the clock frequency of 74.175 MHz from the second PLL 208b.

Also, when an NTSC signal with a frame rate of 59.94 Hz, which is included in the second group, is input via the ADC 204,, the controller 212 controls the switching portion 208c to select the clock frequency of 74.175 MHz from the second PLL 208b. In this case, the video decoder 202 does not operate. Thus, the controller 212 controls the buffer 210 to block the provision of the clock frequency CLOCK to the video decoder 202, such that the clock frequency CLOCK is provided to only the format converter 206 and the OSGM 214.

As described above, the frame rate of an input digital signal is detected and the clock frequency which corresponds to the detected frame rate is provided to only the blocks for the corresponding signal process. Also, in the case where an analog NTSC signal is input, the corresponding clock frequency can be provided to only the blocks for the corresponding signal process. Thus, omission or redundancy in video signal processing can be prevented.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. An apparatus for selectively converting a clock frequency in a digital signal receiver, comprising:

a first phase locked loop;

a second phase locked loop;

a switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal; and

a controller for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of an input digital signal.

2. The apparatus of claim 1, wherein the first phase locked loop generates a clock frequency of 74.25 MHz, and wherein the second phase locked loop generates a clock frequency of 74.175 MHz.

3. The apparatus of claim 1, wherein the input digital signal has a frame rate selected from the group consisting of 60 Hz, 59.94 Hz, 30 Hz, 29.97 Hz, 24 Hz and 23.97 Hz, wherein if the frame rate of the input digital signal is one of 60 Hz, 30Hz and 24 Hz, the controller controls the switching portion to select and output the clock frequency of the first phase locked loop, and wherein if the frame rate of the input digital signal is one of 59.94 Hz, 29.97 Hz and 23.97 Hz, the controller controls the switching portion to select the clock frequency from the second phase locked loop.

4. The apparatus according to claim 3 wherein the clock frequency of the first phase locked loop is 74.25 MHz, and wherein the clock frequency of the second phase locked loop is 74.175 MHz.

5. A digital signal receiver comprising:

a video decoder for decoding a video component of a received digital signal into a first input digital signal;

an analog to digital converter for converting a received analog video signal into a second input digital signal;

a format converter for receiving either of said first and second input digital signals, according to which of said first and second input digital signals is present, said format converter for converting the input digital signal received by said format converter into a predetermined display format output signal;

a controller for detecting a frame rate of the input digital signal received by said format converter and outputting a timing control signal corresponding to the frame rate detected; and

clock frequency providing means for providing a clock frequency according to the timing control signal output by said controller, said clock frequency provided to the format converter for converting the input digital signal received by said format converter into said predetermined display output signal; said clock frequency also provided to said video decoder when said second input digital signal is not present at said format converter.

6. The digital signal receiver according to claim 5, wherein said clock frequency providing means comprises:

a first phase locked loop for generating a first clock frequency;

a second phase locked loop for generating a second clock frequency; and

a switching portion that receives said timing control signal from said controller and said switching portion outputting one of said first and second clock frequencies corresponding to the received timing control signal as said clock frequency.

7. The digital signal receiver according to claim 6, further comprising an on-screen graphics mixer for mixing desired graphics with said predetermined display format output signal to output a mixed graphics video signal, wherein said on-screen graphics mixer operates responsive to the clock frequency provided by said clock frequency providing means.

8. The digital signal receiver according to claim 7, further comprising a video signal processor for processing the mixed graphics video signal output from said on-screen graphics mixer.

9. The digital signal receiver according to claim 7, further comprising audio signal processing means for processing audio signals received in said digital signal receiver.

10. A method of adapting clock frequencies in a digital signal receiver to correspond with a frame rate of an input broadcast signal, said method comprising:

receiving said input broadcast signal into said digital signal receiver;

detecting a frame rate of the input broadcast signal received;

selecting a clock frequency that corresponds to the frame rate which is

detected; and

outputting the clock frequency which is selected to components of the digital signal receiver that use the clock frequency to decode and display said input broadcast signal.

11. The method according to claim 7 wherein the step of selecting the clock frequency comprises, outputting a control signal from a controller, said control signal depending upon the frame rate which is detected; receiving said control signal into a selector, said selector connected to outputs of a plurality of phase locked loops, wherein each phase locked loop has a predetermined clock frequency, and selecting one predetermined clock frequency of one of said plurality of phase locked loops based upon the control signal received by the selector.

Abstract of the Disclosure

An apparatus and method for selectively converting a clock frequency in a digital signal receiver. The apparatus includes: a first phase locked loop (PLL); a second phase locked loop; a switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal; and a controller for controlling the switching portion to select and output the clock frequency corresponding to the frame rate of an input digital signal. The frame rate of an input digital signal is detected and the clock frequency which corresponds to the detected frame rate is provided to only the blocks for the corresponding signal process. Also, in the case where an analog NTSC signal is input, the corresponding clock frequency can be provided to only the blocks associated with the corresponding signal process. Thus, omission or redundancy in video signal processing can be prevented.

FIG. 1

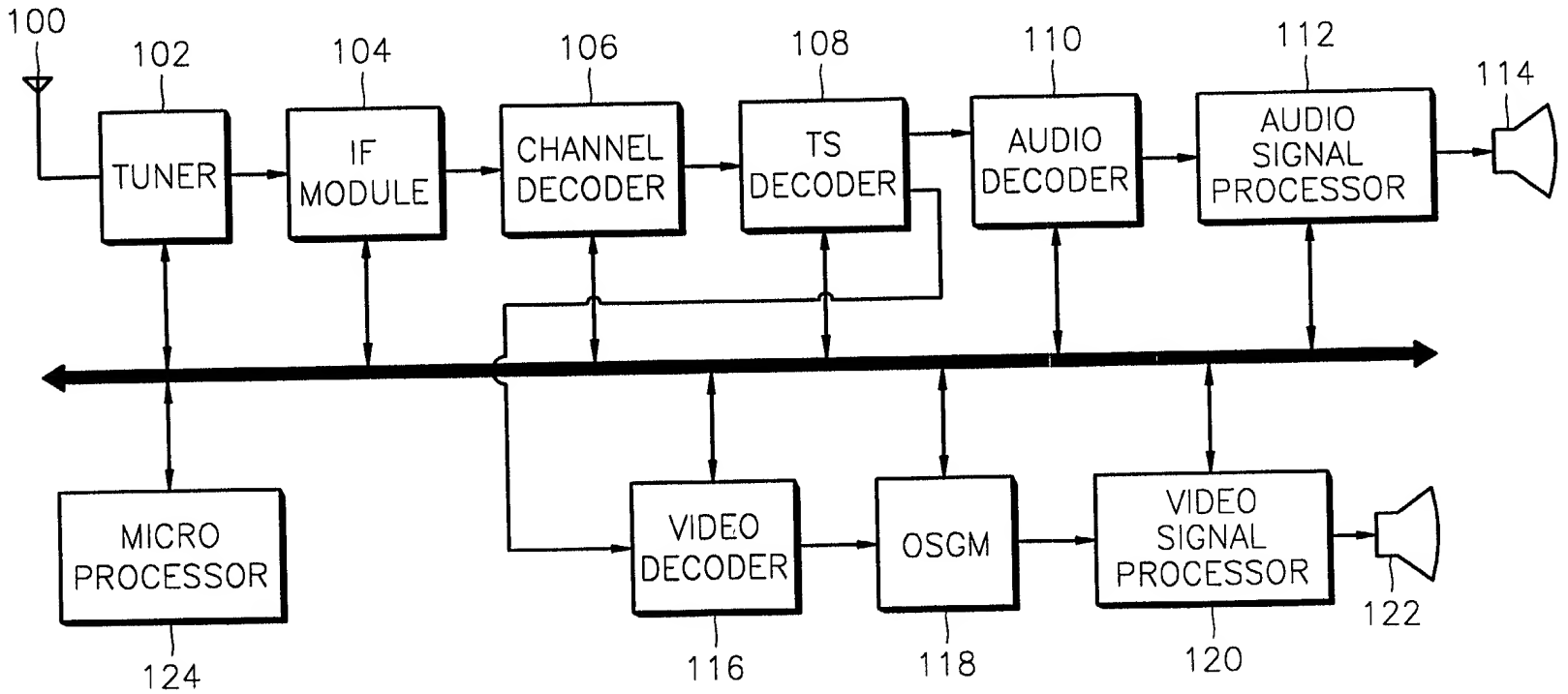
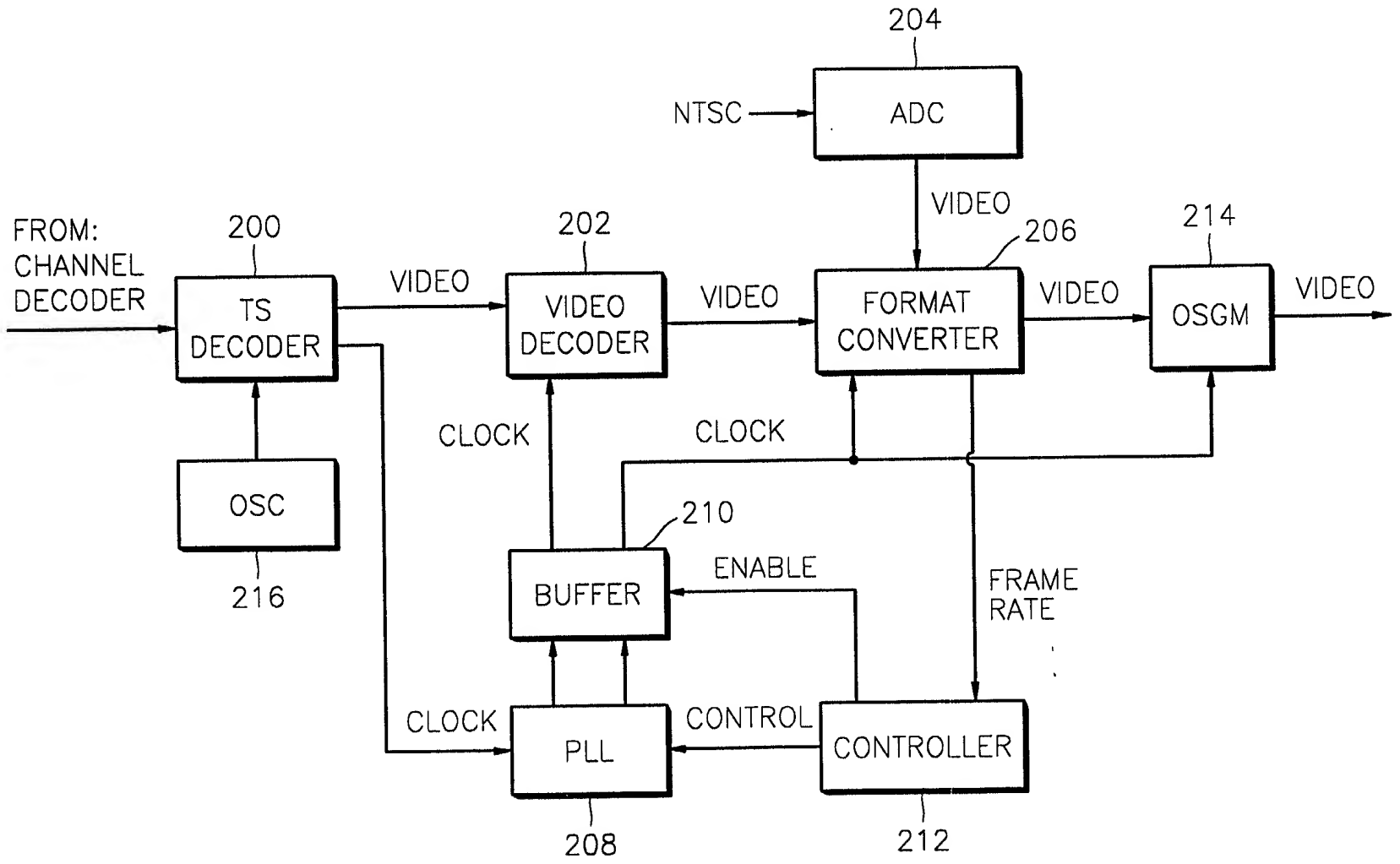

100
102
104
106
108
110
112
114
TUNER
IF MODULE
CHANNEL DECODER
TS DECODER
AUDIO DECODER
AUDIO SIGNAL PROCESSOR
MICRO PROCESSOR
VIDEO DECODER
OSGM
VIDEO SIGNAL PROCESSOR
122
124
116
118
120

FIG. 2


204
NTSC
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CHANNEL
DECODER
200
TS
DECODER
VIDEO
202
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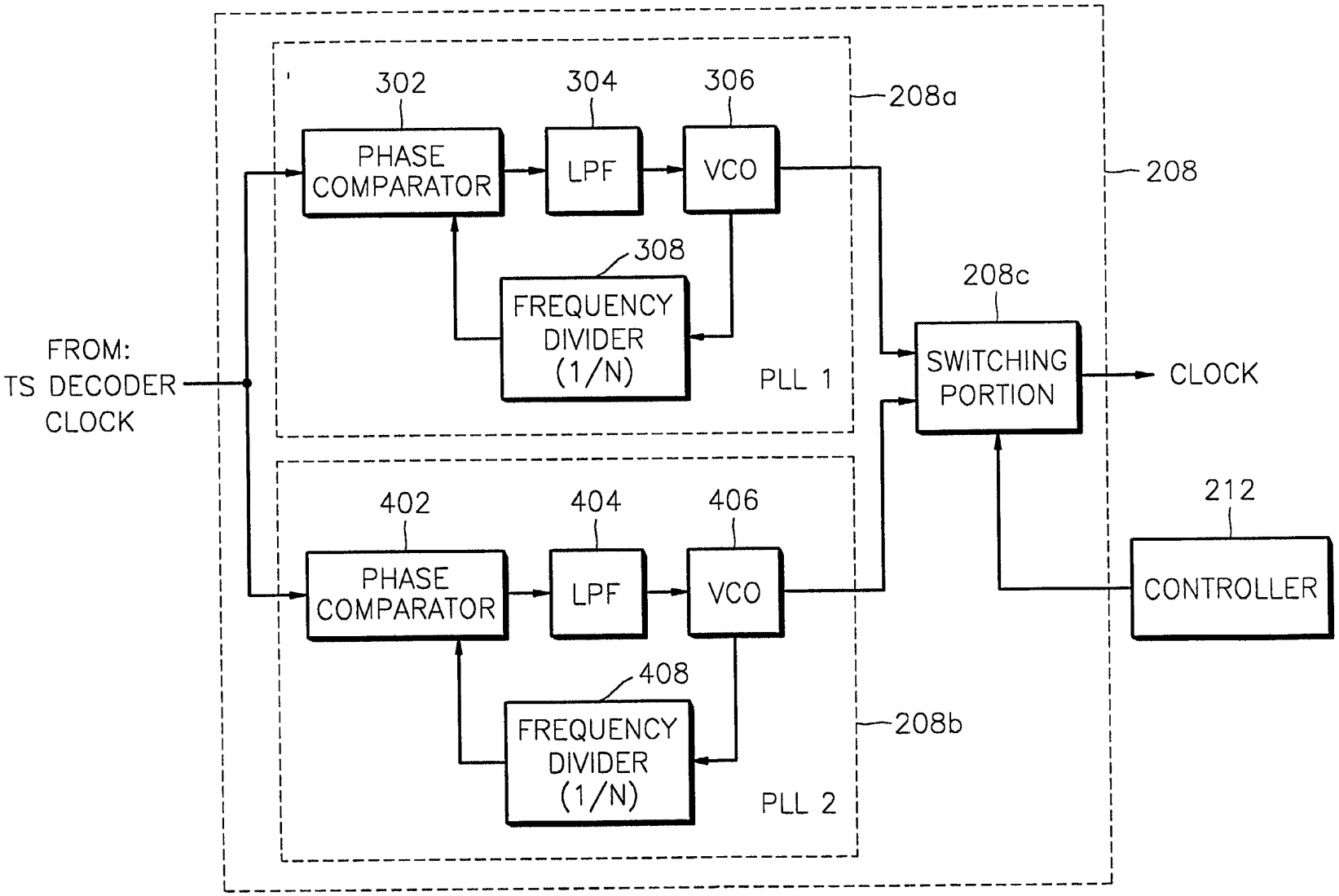
DECODER
VIDEO
206
FORMAT
CONVERTER
VIDEO
214
OSGM
VIDEO
CLOCK
CLOCK
OSC
216
210
BUFFER
ENABLE
FRAME
RATE
CLOCK
PLL
CONTROL
CONTROLLER
208
212

FIG. 3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304
306
208a
PHASE COMPARATOR
LPF
VCO
208
308
208c
FREQUENCY DIVIDER (1/N)
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SWITCHING PORTION
CLOCK
212
402
404
406
PHASE COMPARATOR
LPF
VCO
CONTROLLER
408
FREQUENCY DIVIDER (1/N)
208b
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